RFuW Engineering Ltd.

RFLM-202602LX-299

Two Stage Passive Limiter Module - SMT

Features:

- Surface Mount Limiter Module: 5mm x 8mm x 2.5mm
- Frequency Range: 2 GHz to 6 GHz
- High Average Power Handling : +35 dBm
- High Peak Power Handling: +50 dBm
- Low Insertion Loss: 0.8 dB
- Low Flat Leakage Power : 18 dB
- Low Spike Energy Leakage: 0.3 ergs
- Recovery Time: 100 nsec
- No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-202602LC-299 SMT Silicon PIN Diode Limiter Module offers both High Power CW and Peak protection in the 2 GHz to 6 Ghz frequency range. It is based on a proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The RFLM-202602LC-299 offers excellent thermal characteristics in a compact, low profile 8mm x 5mm x 2.5mm package. The RFLM-202602LC-299 is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the 2 GHz to 6 GHz frequency range.

The limiter RF circuit characteristics provide outstanding passive receiver protection (always on) which protects against High Average Power up to +35 dBm and High Peak Power up to +50 dBm pulsed (pulse width = 1 usec, duty cycle = 0.1%) while maintaining low flat leakage to less than 18 dBm (typical), and reduces Spike Leakage to less than 0.3 ergs.

ESD and Moisture Sensitivity Rating

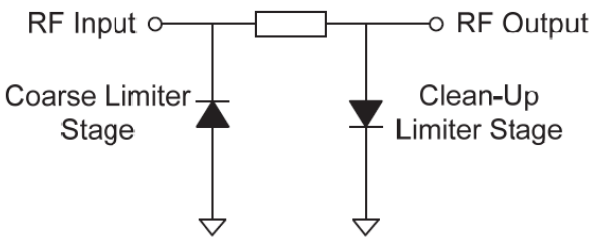
The RFLM-202602LC-299 Limiter Module carries a Class 1 ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

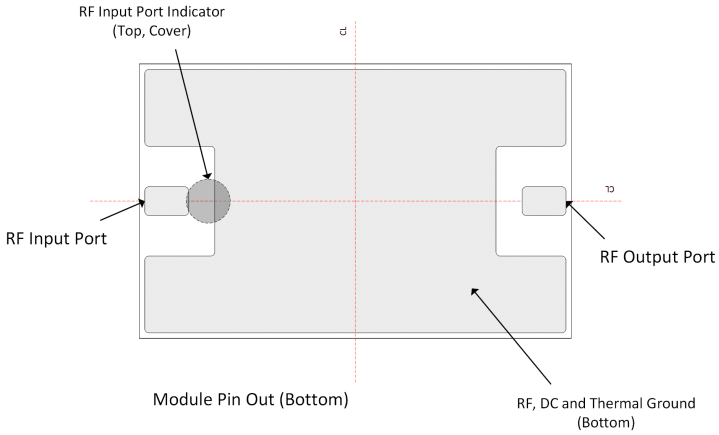
The RFLM-202602LC-299 substrate has been design to offer superior long term reliability in the customer's application by utilizing a proprietary design methodology has minimized the thermal resistance from the PIN Diode junction to base plate (R_{THJ-A}) to less than 40°C/W. Also, ultra-thin Au plating to combat Au embrittlement concerns.

This two stage limiter design employs a second stage limiter and quarter wavelength spacer detector circuit which permits ultra-fast turn on of the High Power PIN Diodes. This circuit topology couple with the thermal characteristic of the substrate design enables reliably handling High Input RF Power up to +35 dBm CW and RF Peak Power levels up to +50 dBm (1 uSec pulse width @ 0.1% duty cycle with base plate temperature at 85°C).

RFLM-202602LC-299 Limiter Module Schematic - No RF Coupling Capacitors



Pin Out



Absolute Maximum Ratings

@ Zo=50Ω, T_A= +25°C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}=85°C, source and load VSWR < 1.2, RF Pulse width = 1 usec, duty cycle = 0.1%, derated linearly to 0 W at T_{CASE}=150°C (See note 1)	+50 dBm
RF CW Incident Power		+35 dBm
θ_{JC} Thermal Resistance		40°C/W
Assembly Temperature		260°C for 30 seconds

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

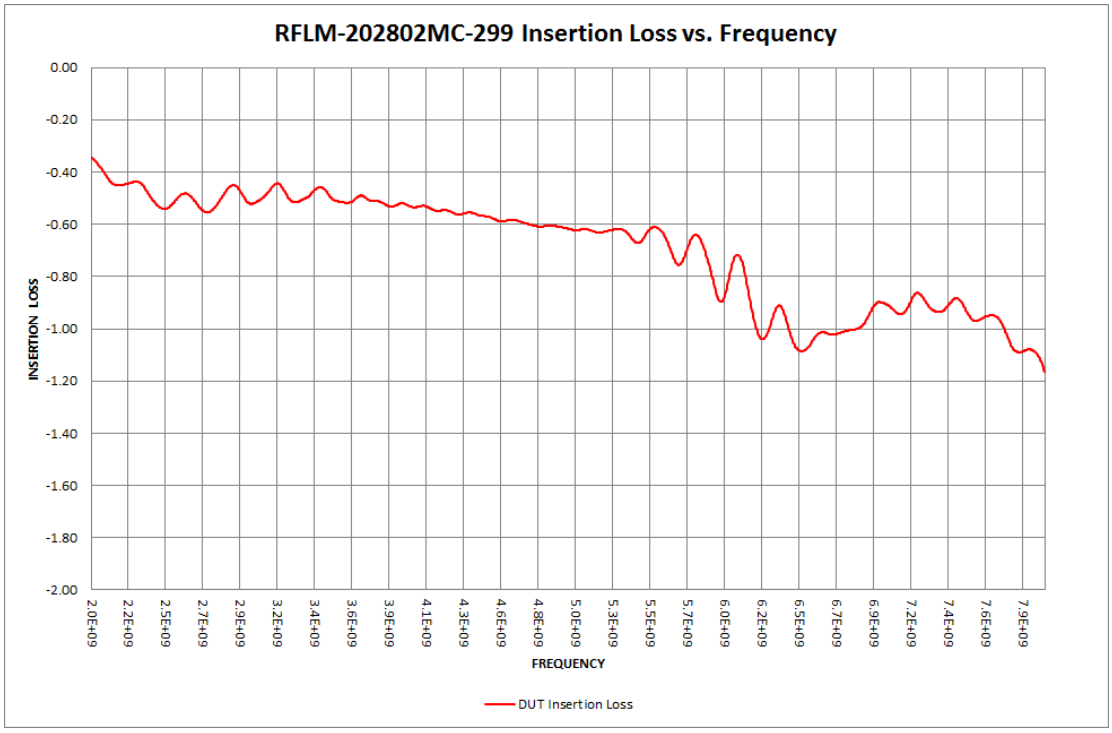
RFLM-202602LC-299 Electrical Specifications

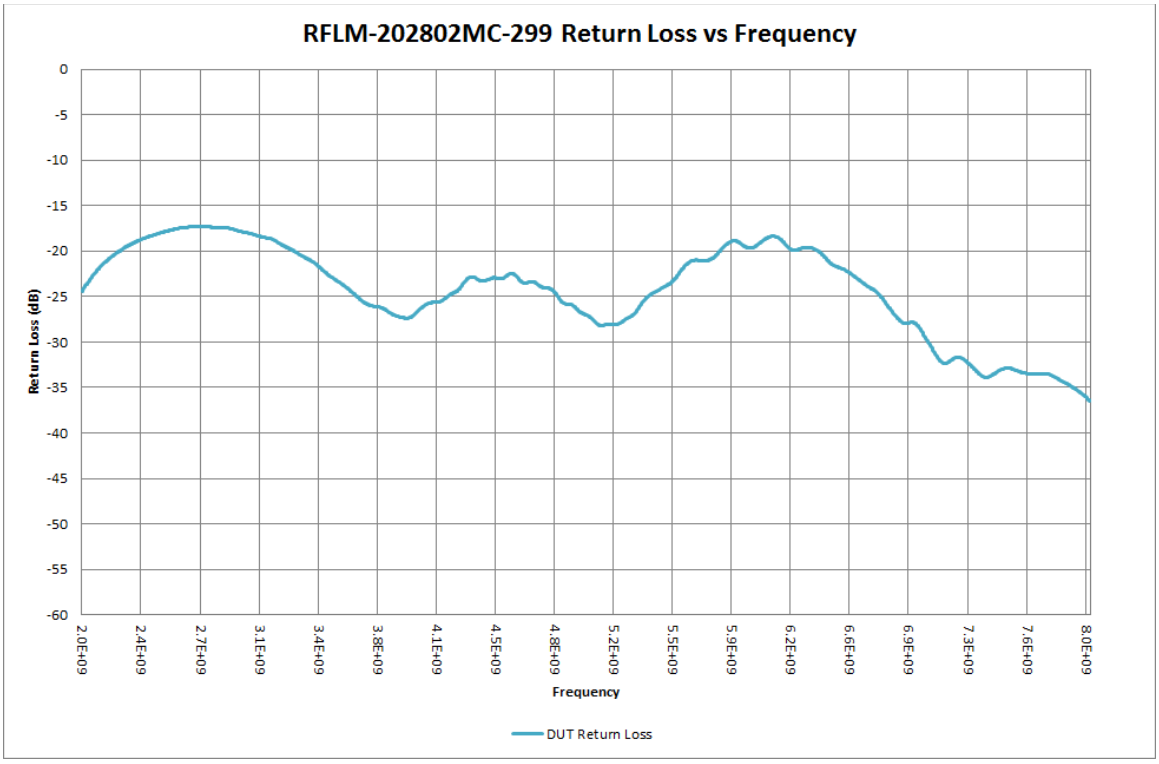
@ Zo=50Ω, TA= +25oC as measured on the base ground surface of the device.

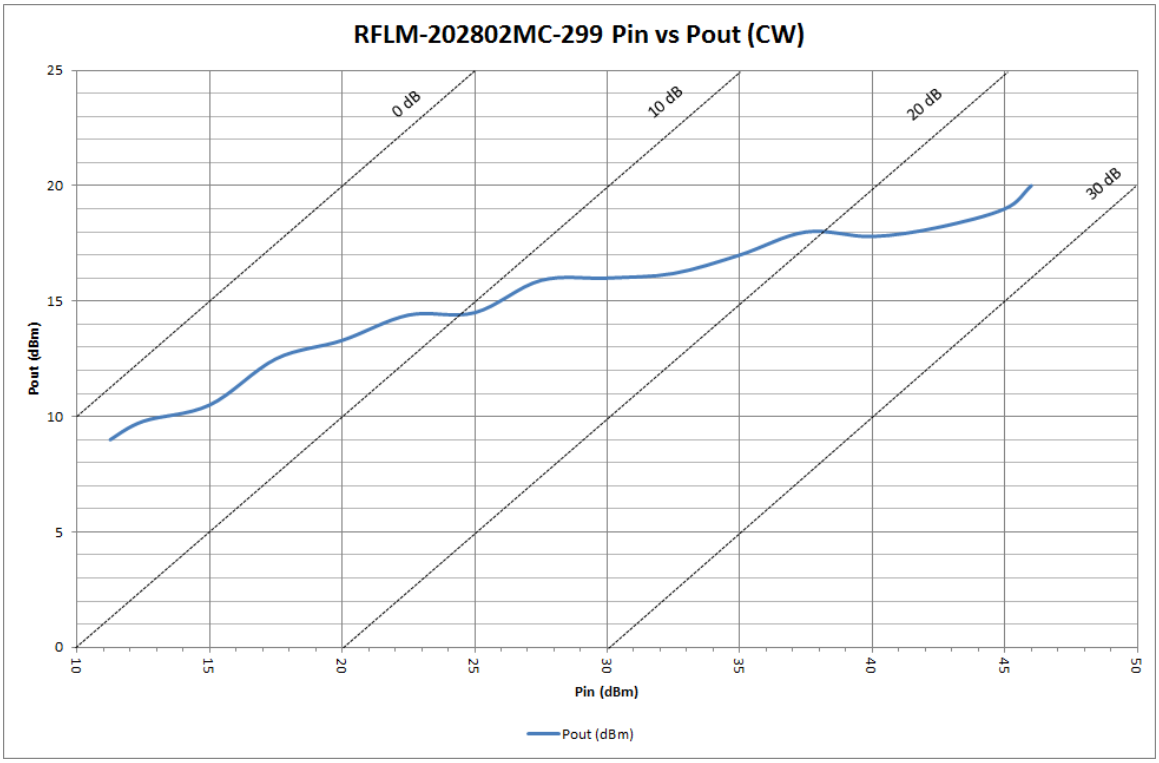
Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F		2.0		6.0	GHz
Insertion Loss	IL	2 GHz ≤ F ≤ 6 GHz, P_{in}= 0 dBm		0.8	1.1	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	2 GHz ≤ F ≤ 6 GHz, Pin ≤ -10 dBm		0.005		dB/°C
Return Loss	RL	2 GHz ≤ F ≤ 6 GHz, Pin= 0 dBm	13	14		dB
Input 1 dB Compression Point	IP_{1dB}	Swept Frequency	7	8	10	dBm
2nd Harmonic	$2F_o$	P_{in}= 0 dBm, F_o = 2.0 GHz	45	50		dBc
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 1 usec, duty cycle = 0.1%, t_{rise} ≤ 2us, t_{fall} ≤ 2 usec		50	51	dBm
CW Incident Power	$Pi_{nc(CW)}$	2 GHz ≤ F ≤ 6 GHz		35	36	dBm
Flat Leakage	FL	P_{in} = 50 dBm, RF Pulse width = 1 us, duty cycle = 0.1%, t_{rise} ≤ 2 us, t_{fall} ≤ 2 us		18	20	dBm
Spike Leakage	SL	Pin = 50 dBm, RF Pulse width = 1 us, duty cycle = 0.1%		0.1	0.2	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = 50 dBm peak, RF PW = 1 us, duty cycle = 0.1%, trise ≤ 2us, t_{fall} ≤ 1 usec		100	150	Nsec

RFLM-202602LC-299 Typical Performance

Z_o = 50Ω, T_{CASE} = 25°C, PIN = 0 dBm as measured on the Ground Plane of the device.

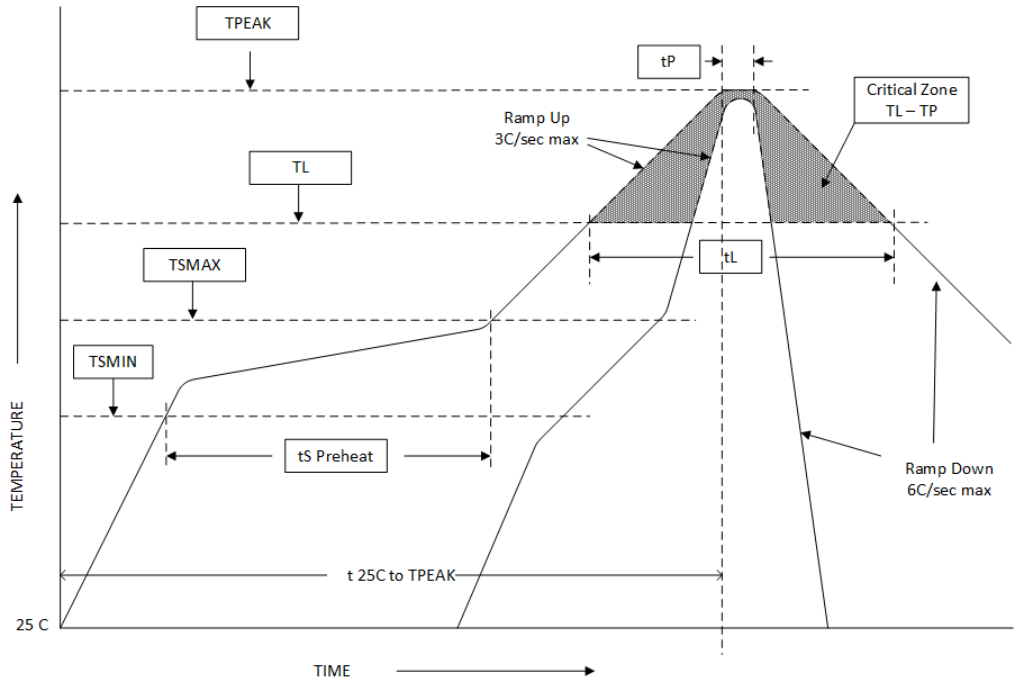




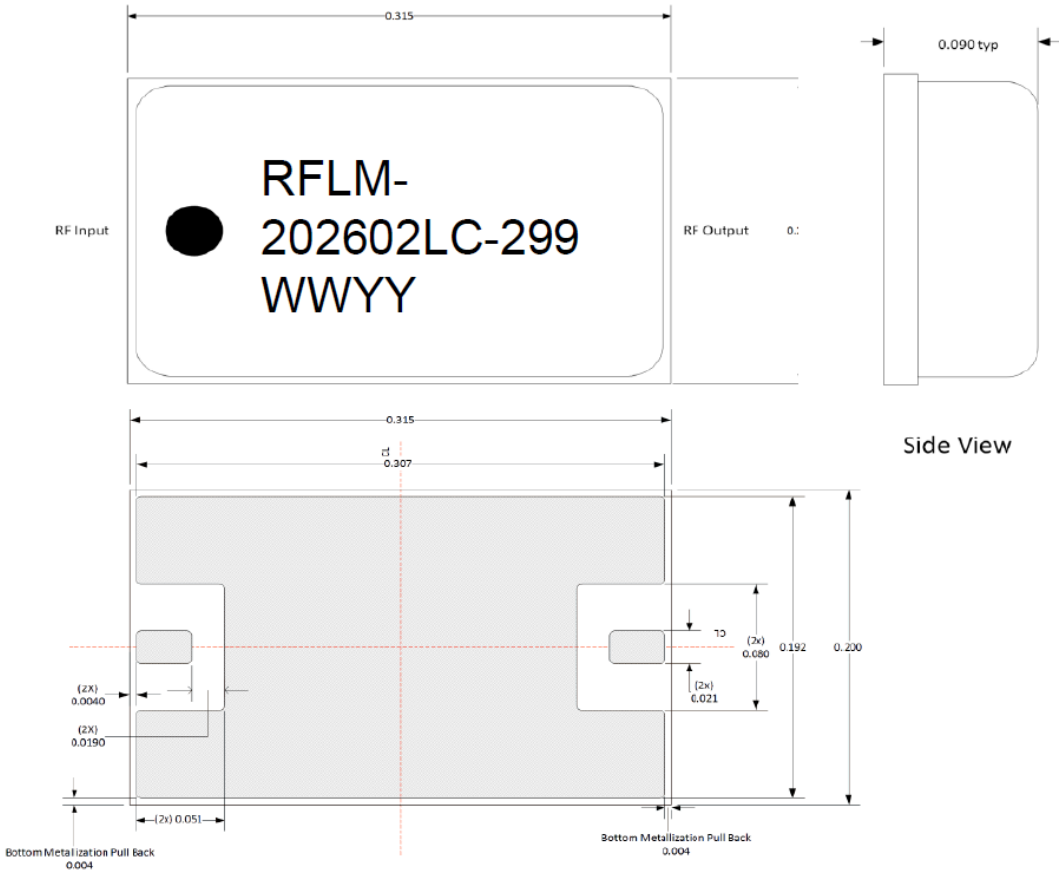


Time-Temperature Profile

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 120 sec
T_{smax} to T_L Ramp up Rate	 	 3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)



RFLM-202602LC-299 Limiter Module Package Outline Drawing



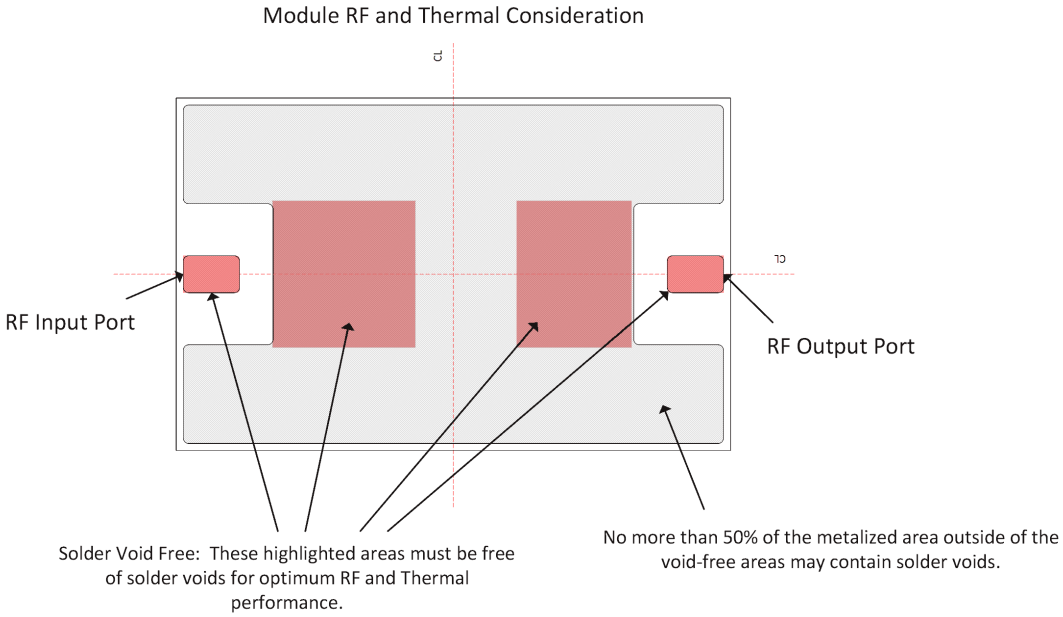
Notes:

1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (15 u in typ Au plated over Ti-Pd).

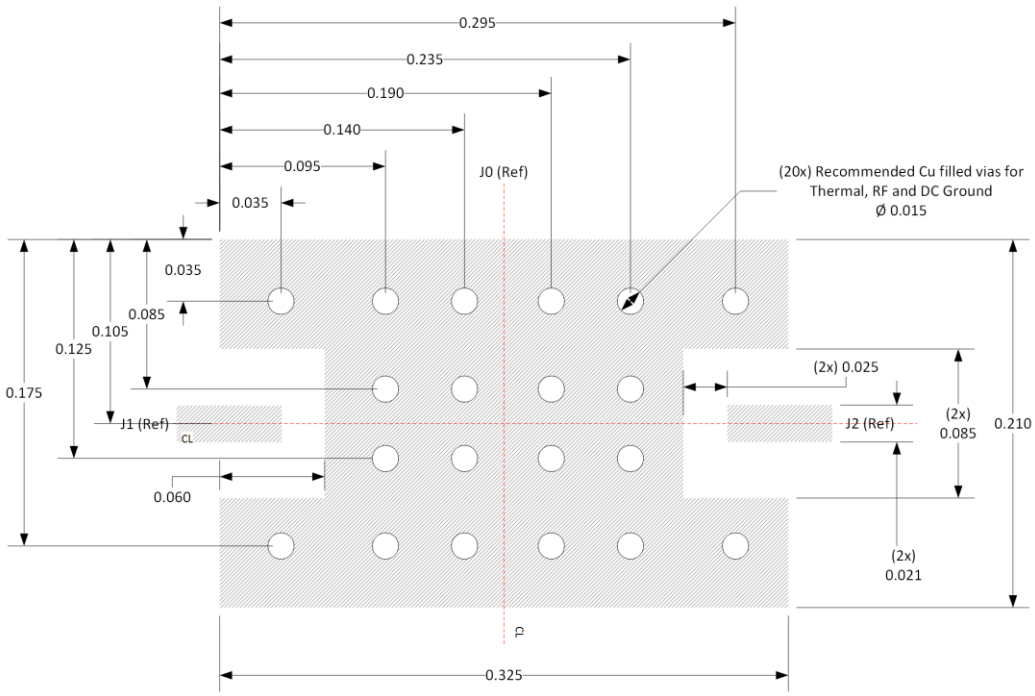
Thermal Design Considerations:

The design of the RFLM-202602LC-299 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature to less than 85°C.

There must a minimal thermal and electrical resistance between the limiter and ground. Adequate thermal management is required to maintain a T_{jc} at less than +175°C and therefore will not adversely affect the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.



Recommended RF Circuit Solder Footprint for the RFLM-202602LC-299



Notes:

1) Recommended PCB material is rogers 4350, 10 mils thick.
2) Hatched area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.
3) All dimensions in inches.

Part Number Ordering Detail:

The RFLM-202602LC-299 Limiter Modules are available in either tube or Tape & Reel format.

Part Number	Description	Packaging
RFLM-202602LC-299	2 GHZ – 8.0 GHz Frequency Band Limiter, No DC Blocking Caps	Tube
RFLM-202602LC-299TR	2 GHZ – 8.0 GHz Frequency Band Limiter, No DC Blocking Caps	TR (250 pcs)